rp8400 / rp7410 / rp7405 and Server Expansion Unit (SEU) Firmware Update Release Notice V6.4

Contents

Caution: Installation of firmware version 6.0 or later on a system using vPars software revision A.02.02 may cause the virtual partition to not boot. Ensure that rp8400 and rp7410/rp7405 systems utilizing vPars software revision A.02.02 **do not** upgrade firmware to version 6.0 or later.

HP Restricted

04/04/2005

Document Revision 1.0

Caution: Read this document in its entirety prior to performing Firmware Update Procedures.

Announcements

This release notice provides information and installation/upgrade instructions for the rp8400, rp7410/rp7405 and Server Expansion Unit (SEU) Firmware Release Version 6.4.

The following new features were added in MP version 4.022:

- None

The following new features were added in PDC version 17.009:

- New IODC drivers were added for support of AB290, AB465, AB545 I/O Cards

Revisions to this Document

Component	**Version 1.0 rp8400 only** Released 9/6/2001	**Version 2.0 rp8400 only** Released 1/9/2002	**Version 3.01** Released 4/9/02	**Version 4.0 or 4.11 4.0 Released** 8/01/02 **4.1 Released** 9/13/02	**Version 5.0** Released 03/17/03
System Backplane					
GPM	1.00 or 1.02	1.00 or 1.02	1.02	1.002	1.002
FM	1.01 or 1.02	1.01 or 1.02	1.02	1.002	1.002
OSP	1.00 or 1.01	1.00 or 1.01	1.01	1.001	1.001
PCI Backplane					
LPM	1.00 or 1.02	1.00 or 1.02	1.02	1.002	1.002
HS	1.00	1.00	1.00	1.000	1.000
Cells					
LPM	2.01	2.01	2.01or 2.002	2.002	2.002
BOB	1.00	1.00	1.00	1.000	1.000
Drain	1.00	1.00	1.00	1.000	1.000 or 1.001
SINC	1.09	1.12	2.00	2.002	2.002
PDC	13.010	14.005	15.007	16.009	16.011
Core IOs					
CIO	1.00	1.00	1.00	1.001	1.001
MP	1.09	1.14	2.08	3.005	4.009
Processors					
CPU	PA-8700 Revision 2.2 750 MHz	PA-8700 Revision 2.2 650 & 750 MHz	PA-8700 Rev. 2.2/2.3 650 & 750 MHz	PA-8700 650 MHZ Rev. 2.2/2.3 750 MHZ Rev. 2.2/2.3 750 MHZ Rev. 3.0/3.1 875 MHZ Rev. 3.0/3.1	

Component	**Version 6.0** Released 09/05/03	**Version 6.1** Released 12/10/03	**Version 6.2 Released 2/09/04**	**Version 6.3 Released 4/21/04**
System Backplane				
GPM	1.002	1.002	1.002	1.002
FM	1.002	1.002	1.002	1.002
OSP	1.002	1.002	1.002	1.002
PCI Backplane				
LPM	1.002	1.002	1.002	1.002
HS	1.000	1.000	1.000	1.000
Cells				
LPM	2.002	2.002	2.002	2.002
BOB	1.000	1.000	1.000	1.000
Drain	1.001	1.001	1.001	1.001
SINC	2.002	2.003	2.004	2.004
PDC	17.005	17.006	17.006	**17.008**
Core IOs				
CIO	2.008	2.008	2.008	2.008
MP	4.013	4.015	4.018	**4.020**
Processors				
CPU	PA-8700 650 MHZ Rev. 2.2/2.3 750 MHZ Rev. 2.2/2.3 750 MHZ Rev. 3.0/3.1 875 MHZ Rev. 3.0/3.1			

Note: The drain firmware file **(`drain_1.1.0b.osp`)** Version 1.001 can be used on systems with Version 5.0 or Version 6.X installed.

Component	Version 6.4 Released 04/04/05
System Backplane	
GPM	1.002
FM	1.002
OSP	1.002
PCI Backplane	
LPM	1.002
HS	1.000
Cells	
LPM	2.002
BOB	1.000
Drain	1.001
SINC	2.002
PDC	**17.009**
Core IOs	
CIO	2.008
MP	**4.022**
Processors	
CPU	PA-8700 650 MHZ Rev. 2.2/2.3 750 MHZ Rev. 2.2/2.3 750 MHZ Rev. 3.0/3.1 875 MHZ Rev. 3.0/3.1

Note: The drain firmware file **(`drain_1.1.0b.osp`)** Version 1.001 can be used on systems with Version 5.0 or Version 6.X installed.

Known Problems and Workarounds

1. Use vPar software version A.02.03 or later when running on rp8400 or rp7410/rp7405 systems.

   Caution: Installation of firmware version 6.0 or later on a system using vPars software revision A.02.02 may cause the virtual partition to not boot. Ensure that rp8400 and rp7410/rp7405 systems utilizing vPars software revision A.02.02 **do not** upgrade firmware to version 6.0 or later.

2. A6795A single-port PCI 2 GB fibre-channel adapters cannot boot from XP256 connected through Hub.
3. A6795A single-port PCI 2 GB fibre-channel adaptors cannot boot from XP512 either in direct attach or connected through Hub.
4. Due to a software issue, the attention LED will be turned on for empty slots on a VPar reboot. The slot will remain functional and will allow on-line addition of PCI cards. Under these conditions, the LED does not indicate a hardware failure. In a VPars environment, the LED state for an empty slot should be ignored.
5. When a user has two or more console windows open into a system and types <control s> in one window to stop scrolling, then reboots the system in another window, the reboot will stall prior to reaching the BCH prompt. The user will receive no indication as to why the system has stalled. To recover from this, the user must type <control q> in the same window that the <control s> was typed, close this window, or reboot the manageability processor.
6. Use of the Genesis profile command at the MP command menu returns Invalid Sequence IDs for complex profile groups B and C. This result is expected, but users will note a MP error log entry resulting from this command.
7. Chassis code errors may appear in the MP error log. This problem may manifest itself as an orphan chassis code (ORPHAN_CC log entry) or an error level 13 entry.
8. When updating MP firmware from version 2.08 (Version 3.01) or version 3.005 (Version 4.0/4.11) to 4.022 (Version 6.4) the MP LAN configuration will be overwritten with default values. Before updating the MP firmware, execute the MP command 'ls' to document the LAN's configuration. Upon completion of a successful MP 4.022 version update, it is necessary to connect a serial console and execute the MP 'lc' command to reconfigure the MP LAN.
9. When an rp7405/rp7410, rp8400 or Server Expansion Unit (SEU) has a failed fan and the chassis is powered off, the fan will not report as failing when the chassis is powered on.
10. In a 2-cell single-partition rp7405 / rp7410 system, the Service Menu's "LanAddress" command will return the LanAddress of the root cell's Core LAN only; it does not return the secondary LAN address of the

partition. This only affects the display of the MAC address of the secondary LAN; it does not affect igniting the system or normal boot of the system. The secondary LAN works normally under HPUX.

Fixes in this Version

1. PDC revision 17.009 contains the following fixes:

- An intermittent problem could occur during boot up where one or more cells were caught in an infinite loop reporting a chassis code of BOOT_UNEXPECTED_INTERRUPT. Firmware was modified to eliminate this intermittent problem.
- During performance measurements of a Procurium Core I/O card in an rp7410, it was discovered that a data buffering control register was not optimally programmed. This was updated and has improved LAN traffic performance.
- VPAR monitor panic when shutting down or rebooting a VPAR after aborting a PCI OLR operation. Firmware has been modified to resolve this issue.
- When an IO Bus or Rope or Rope-Unit or Link has gone fatal, a high-alert level chassis code is logged. The chassis code information has been expanded to include all the physical location information (chassis, bay, slot).

2. MP revision 4.022 contains the following fixes:

- A possibility exists on rp7410/7405 system with two Core I/O's installed allowing both Core I/O's to be configured as the Master. This condition is timing related. When it occurs both Core I/O's will have the Master LED illuminated. Firmware was modified to allow only one Core I/O to be configured as the Master.

Firmware Update Information, Precautions and Warnings

1. Firmware files may be obtained from several locations. When downloading firmware files, all files should be stored in the same location (path). This allows a firmware update of all entities during one firmware update session.

   NOTE: Always download the files to your PC in Binary Mode

2. Outside the HP firewall, files may be located via Web browser at:

   Note: The following bundle contains the combined rp8400 / rp7410/rp7405 firmware files and updated release notes. Firmware updates should be performed by qualified support personnel.

   ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CKEYMAT0604.tar.gz.txt

   And

   ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CKEYMAT0604.tar.gz

   Inside the HP firewall, the new files are available at:

   Note: The following bundle contains the combined rp8400 / rp7410/rp7405 firmware files and updated release notes. Firmware updates should be performed by qualified support personnel.

   ftp://hpatlse.atl.hp.com/firmware_patches/hp/cpu/PF_CKEYMAT0604.text

   And

   ftp://hpatlse.atl.hp.com/firmware_patches/hp/cpu/PF_CKEYMAT0604.tar.gz

3. The following tools will be required for firmware updates:

   - Network console connection to a MP console port.
   - Laptop and 9 pin RS-232 serial cable if network console is not available.
   - Windows XP or HP-UX FTP server with firmware file from sites listed above.

     Note: Information about configuring a Windows XP FTP server can be obtained on an internal WTEC website at: http://wtec.cup.hp.com/~cpuhw/hppa/rp8400/firmware/ftp-server.doc

4. The file names on all FPGA files have been changed from .bin extensions to .osp extensions. The file names changed to reflect new FGPA hardware that was incompatible with the old programming method. The new .osp files

can upgrade the existing FPGAs on the current products and their replacements that will show up on new products as the current FPGA's are discontinued by their manufacturer. These files are compatible with the same OSP utility as before.

5. *Do not attempt to update PDC firmware on a partition with the Operating System running*. The Firmware Update Utility puts the PA processors into a reset condition, which will cause HP-UX to crash.

> **Note:** If an Operating System is up and running on a cell board the following warning will now be generated, please follow the warning instructions:
>
> ```
> Cell board 0 may have a booted OS running on it.
> Updating PDC on this cell board will crash the OS.
> Enter quit at the next prompt if you wish to abort
> this session, shut down the partition and restart.
> ```

6. The SINC and MP firmware can be updated with 48V power *on* or *off* to the machine. The PDC firmware update requires 48V power to be *on* for each cell requiring an update. Verify power status using the PS command as shown in Step 2 of the following section titled *rp8400 Firmware Update Procedure Using Anonymous FTP Server.*

7. It is not necessary for a cell board to be joined to a partition to perform a PDC or SINC update on that cell board.

8. SINC and MP firmware upgrades require a *reset*. This reset is performed at the MP Command Menu prompt. PDC upgrades *do not* require a reset.

9. Multi-partition machines may now operate each partition at different CPU frequencies (e.g., Partition 0 operating at 750 MHz with Partition 1 operating at 875 MHz). However, each partition must operate at the same firmware version, and the processors in each partition must be capable of operating at the same speed.

10. 875 MHz PA-8700 version 3.0 and 3.1 processors may be used in partitions operating at 650, 750 or 875 MHz. Operating speed is determined by cell board dipswitch settings.

11. 750 MHz PA-8700 version 2.2, 2.3, 3.0 & 3.1 processors may be used in partitions operating at either 650 or 750 MHz. Operating speed is determined by cell board dipswitch settings.

12. 650 MHz PA-8700 version 2.2 and 2.3 processors may only be used in partitions operating at 650 MHz. Operating speed is determined by cell

board dipswitch settings.

13. The terms *upgrade* and *update* are used synonymously. The acronyms *SINC* and *PDHC* are also used synonymously.

14. When updating cell or core IO boards equipped with Version 1.0 firmware to Version 6.4, certain restrictions exist. These conditions are listed under the *System Board Compatibility* section of this document.

15. Users updating system FPGAs from firmware Version 1.0 or Version 2.0 must update the System Backplane OSP FPGA to Version 4.0/4.11 prior to subsequent FPGA firmware updates. Following the OSP FPGA update, an AC power cycle is required. Users with multi-partition configurations should note that power must be cycled for all partitions.

16. On the rp8400 server only, updates of cell FPGAs using the OSP Utility, requires the use of a scree board (HP P/N 1253-5394) mounted at connector J-22 of the system backplane board.

17. The following warning is issued during cell board FPGA updates using the OSP Utility to remind users that a scree board may be required:

```
WARNING:  This system MAY lack the hardware connectivity
necessary to allow updating of FPGA's on the cell boards!
```

18. The rp8400 and the rp7410/rp7405 DO NOT use the same CIO file when updating the FPGA. The File for the rp8400 is "cio2.8.0b.osp" and the file for the rp7410/rp7405 is "matcio_2.8.0b.osp". If an attempt is made to download the wrong file an error message will be generated.

19. The version displayed in the OSP software utility banner is not the version of the FPGA firmware; it is the version of the OSP software utility. To view the FPGA firmware revision use the MP sysrev command.

System Board Compatibility

The rp8400 and rp7410/rp7405 systems contain four replaceable boards equipped with flash memory or FPGAs. These include the system backplane, PCI backplane, cell, and core IO/MP.

In the event that board replacement is necessary, it is possible that replacement boards will not be equipped with matching firmware upon arrival. Currently, the rp8400 and rp7410/rp7405 do not support operation with multiple firmware revisions (either within a partition, or across multi-partition machines). Therefore, the new board must be 'upgraded' or 'downgraded' to match the existing machine firmware version.

These updates contain restrictions (Notes 1 & 2 is listed below see rp8400 restrictions) (Note 3 is listed below see rp7410/rp7405 / rp8400 restrictions). All other updates must be performed per the applicable Release Notice, which may contain additional restrictions.

All new boards may be 'updated' to all existing machine firmware versions using the applicable procedure (for example, customers with existing machine firmware Version 3.01 would use *rp8400 Firmware Update Release Notice V3.01*). System board compatibility restrictions will be listed in the *System Board Compatibility* section, if restrictions exist.

rp8400 restrictions

When updating cell or core IO boards equipped with Version 1.0 firmware to Version 6.4, the following conditions exist:

> **Note 1:** Cell boards cannot be powered on and PDC cannot be updated until the MP is updated to revision MP 3.005, which is only available in Version 4.0/4.11. Therefore, the MP must be updated and reset prior to updating PDC.
>
> **Note 2:** Following this MP update to revision MP 3.005, the cells must be powered on using the front power switch on the machine in lieu of the PE command at the Command Menu prompt.

rp7410 / rp7405 / rp8400 restrictions

When updating core IO boards equipped with Version 3.01 or Version 4.0/4.11 firmware to Version 6.4, the following condition exists:

> **Note 3:** LAN Parameters will be lost when updating to V6.4. This behavior occurs due to a change in data storage location for the Manageability Processor firmware.

Prior to updating a core IO from an older version to V6.4, record the following LAN Parameters using the **MP:CM>lc** command: IP Address, Hostname, Subnet Mask and Gateway.

Following MP firmware update, a reset is performed. At this point, LAN Parameters are lost, and access to the MP Command Menu settings is only available via local serial console.

Upon first login through the local serial console, reset the master MP via **MP:CM>xd>3**. Following MP reset, login again through the local serial console and enter the recorded IP Address, Hostname, Subnet Mask and Gateway information using the **MP:CM>lc** command. LAN Parameters are now preserved through future reboots or removal of power.

rp7410 / rp7405 / rp8400 processor and firmware compatibility

There are now two types of CPU chips for these products, version 3.x (3.0 & 3.1) and version 2.x (2.2 & 2.3). They also come in different speeds, 650 MHz (version 2.x only), 750MHz and 875MHz. Here are the rules:

1. Version 3.x CPU chips require Firmware release 4.0/4.11 as the minimum release version installed. No exceptions…
2. If a version 3.x CPU chip is installed in a system that does not have firmware release 4.0/4.11as the minimum release version installed, the CPU will not rendezvous with the partition. (See rule 1)
3. Version 2.x and 3.x CPU chips can be mixed on the same Cell board. (See rule 1)
4. All Cells in a given partition must be set for the same speed using the dipswitches on the Cell board.
5. A complex can have different partitions running at different speeds. For example, one partition running with 875MHz CPU's and a different partition running on 750MHz CPU's.
6. 875MHz and 750MHz CPU chips can be installed on the same Cell board but the speed setting of the Cell board must be set to correspond to the slowest CPU installed in the Cell board.
7. There is no physical way to tell the difference between a version 2.x 750MHZ chip and a version 3.x 750MHz CPU chip. The only way to tell is to install the CPU on a Cell and use the MP:CM>df command to check the version number of the CPU. (See note below)

Note: Because there was not a part number change AND there is no physical way to tell the difference between a version 2.x 750MHZ chip and a version 3.x 750MHz CPU chip, a label has been added to the new 3.x 750 MHZ processors, so that we can easily determine what version of CPU has been received and if a complete firmware upgrade is required to accept a replacement processor.

This label will be on the outside of the box AND inside the box on the anti-static bag.

If you receive a 750MHZ CPU and there is no identification label, you will still have to use the information provided in items 1 - 7 to determine what version of processor you received.

rp8400 / rp7410 / rp7405 Firmware Update Procedure Using the Firmware (FW) Update Utility

Note 1: The firmware update process requires file transfer via telnet session. In the event that a loss of telnet session occurs, and the source of the interruption is corrected within approximately 3 minutes (for example, a removed LAN cable is re-inserted), the Firmware Update Utility will continue automatically with no loss of data.

For interruptions greater than approximately 3 minutes, the Firmware Update Utility will timeout and end, returning the user to the command menu prompt:

```
Command interface inactivity timeout.  Aborting command.

MP:CM>
```

In the case of a timeout and incomplete firmware update, the user must restart the firmware update. DO NOT PERFORM ANY SORT OF RESET, OR POWER CYCLE, UNTIL THE FIRMWARE IS SUCCESSFULLY UPDATED. Failure to do so will result in flash memory corruption.

Note 2: For a machine containing a full compliment of boards, the firmware update session will take approximately 2-1/2 hours for an rp8400 and 1-1/2 hours for an rp7410/rp7405. This time includes power cycles for the FPGA upgrades.

Table 1:

Entity	Approximate Time each (in minutes)
MP	10
PDC	22
PDHC/SINC	3
FPGAs	
OSP	3
GPM	2
FM	2
CIO [1]	3
PCILPM	2
Cell LPM	2

[1] **Remember that there are two CIO files. One for the rp8400 (cio_2.8.0b.osp) and one for the rp7410/rp7405 (matcio_2.8.0b.osp). If you attempt to load the wrong one you will get an error message and the update will abort.**

Step 1 The following conditions are required to perform firmware updates:

- If all entities are to be updated, ensure the Operating System is shutdown, autoboot and autosearch for all partitions is **NOT** enabled and power (48V) to cabinet and cells is ***on***.

- The Operating System must ***not*** be running. If the Operating System is up, perform a shutdown by the following commands :

```
# setboot –b off
# setboot –s off
# shutdown –h 0
```

- The PDC firmware upgrade requires the power (48V) to be *on* for each cell to be updated. Verify a 'Power OK' status for all populated cells using the PS command:

```
MP:CM> ps

Display detailed status of the selected MP bus device.
The following MP bus devices were found:




+---+----+-----+-------+------+-----------+
|   |    | Sys |       | PCI  | Bulk Pwr  |
|Cab| MP |Bkpln| Cells |Domain| Supplies  |
| # |    |     |0 1 2 3| 0  1 |0 1 2 3 4 5|
+---+----+-----+-------+------+-----------|
| 0 | *  |  *  |* * * *| *  * |* * * * * *|
+---+----+-----+-------+------+-----------+

You may display detailed power and hardware status for the
following items:

    T - Cabinet
    S - System Backplane
    G - MP (Core I/O)
    P - PCI Domain
    C - Cell
        Select Device: t

HW status for rp8400 cabinet : NO FAILURE DETECTED

Power switch is on
Right Door is closed
Top Door is closed
Left Door is closed

Total Power Available 6000 VA
Total Power Needed 3768 VA
Power Redundancy : redundant
Power Viability : viable
```

```
 Power Status
---------------+-----+-------+------+-----------+
               | Sys |       | PCI  | Bulk Pwr  |
               |Bkpln| Cells |Domain| Supplies  |
               |     |0 1 2 3| 0  1 |0 1 2 3 4 5|
---------------+-----+-------+------+-----------|
 Populated     |  *  |* * * *| *  * |* * * * * *|
 Enabled       |  *  |* * * *| *  * |* * * * * *|
 Power OK      |  *  |* * * *| *  * |* * * * * *|
 Warning/Fault |     |       |      |           |
 Attention LED |     |       |      |           |
```

Step 2 With power ***on*** to the machine and the Operating System shut down, place the partition(s) in the necessary state for the firmware to be updated. Reset the partition to stop at Boot is Blocked (BIB) by:

```
MP:CM> rr

This command resets for reconfiguration the selected partition.

WARNING: Execution of this command irrecoverably halts all system
         processing and I/O activity and restarts the selected
         partition in a way that it can be reconfigured.


  Part#  Name
  -----  ----
     0)  Partition 0
     1)  Partition 1

    Select a partition number: 0

    Do you want to reset for reconfiguration partition number 0?
   (Y/[N]) y

    -> The selected partition will be reset for reconfiguration.
MP:CM>
```

If you are upgrading the firmware on both partitions you will need to run the "rr" command once again for the other partition.

Step 3 Updating the MP(s):

Note 1:
It is recommended to update the MPs individually. If more than one MP, Update the Slave MP first then the Master. This will enable recovery of the System in the event of a catastrophic failure.

Note 2:
When updating MP firmware from version 2.08 (Version 3.01) or version 3.005 (Version 4.0/4.11) to 4.022 (Version 6.4) the MP LAN configuration will be overwritten with default values. Before updating the MP firmware, execute the MP command 'ls' to document the LAN's configuration. Upon completion of a successful MP 4.022 version update, it is necessary to connect a serial console and execute the MP 'lc' command to reconfigure the MP LAN.

Note 3:
If an SEU is attached, ensure the steps listed in the SEU Firmware Update Procedure section are performed as well.

Launch the Firmware Update Utility:

```
MP:CM> fw
```

Enter the following information when prompted (an example of the Firmware Update Utility screen follows):

```
Enter the Entities to be upgraded:  Select the appropriate
entity/entities to be upgraded.

Enter your user name:  anonymous

Enter your user password:  Enter your e-mail address

Enter the ip address where the firmware can be found:  Enter
the address of the anonymous FTP server.

Enter the path where the firmware can be found:  Enter the
directory path (for example, /dist/version6_4 or some other
location).  Do not list the actual firmware image filenames in
this path.

Enter the filename(s) of the firmware image(s):  For example,
if the MP firmware image is MP_A.4.22.0.bin, enter
MP_A.4.22.0.bin.

Are you sure that you want to continue (Y/N):  y
```

```
MP:CM> fw

    ********************************************************************
    *****                                                          *****
    *****                  Firmware Update Utility                 *****
    *****                                                          *****
    *****       (C) Copyright 2001 Hewlett-Packard Company         *****
    *****                    All Rights Reserved                   *****
    *****                                                          *****
    *****        THIS PROGRAM IS NOT LICENSED TO CUSTOMERS         *****
    *****                                                          *****
    *****  This program is intended for use by trained HP support  *****
    *****  personnel only.  HP shall not be liable for any damages *****
    *****  resulting from unauthorized use of this program.  This  *****
    *****  program is the property of HP.                          *****
    *****                                                          *****
    *****                      Version  3.02                       *****
    *****                                                          *****
    ********************************************************************

                                Protection  Flash        Current
   Number  Cabinet    Name       Domain    Handle   Firmware Version  Comments
   ------ --------- -------- ---------- -------- ------------------ --------
(1)    1         0     MP 0          0        0          4.018       Master
(1)    2         0     MP 1          1        1          4.018       Slave
       3         0   PDHC 0          0      256          2.002          -
       4         0    PDC 0          0      320         16.011          -
```

```
      5         0   PDHC 1          1      257          2.002          -
      6         0    PDC 1          1      321         16.011          -
(2)   7         0   PDHC 2         -1 *    258          2.002          -
(2)   8         0    PDC 2         -1 *    322         16.011          -
(2)   9         0   PDHC 3         -1 *    259          2.002          -
(2)   10        0    PDC 3         -1 *    323         16.011          -
```

(1) On the rp7410/rp7405 server the Master MP is MP1
(2) These entities will only be seen on the rp8400
*** A Production Domain value of –1 indicates that these cells do not belong to a partition.**

```
Enter the Entities to be upgraded (Ex: 3,4,10) : 2
Enter your user name: anonymous
Enter your user password:
Enter the ip address where the firmware can be found: 192.1.1.1
Enter the path where the firmware can be found: /dist/version6_4
Enter the filename of the firmware image for the MP: MP_A.4.22.0.bin
Are you sure that you want to continue(Y/N): y
```

Step 4 Following an update; it is necessary to verify the entity selected was updated successfully. A successful update returns the following message:

```
Firmware Update has completed successfully for all entities.
MP:CM>
```

An unsuccessful update results in an error message. If the FTP connection was successful, but the update failed, a warning will be received for the entity being updated. For example:

```
Firmware Update failed for entity MP 0.
DO NOT REBOOT MP 0 until it has been successfully updated!!!
Firmware Update completed with errors.
```

If more than one MP, perform the firmware update for the other MP as mentioned in Step 3.

NOTE: Re-perform the firmware update procedure immediately for all entities failing to update successfully. DO NOT RESET until you get a message indicating that the update completed successfully.

Step 5 Upon successful completion of the MP firmware upgrade, a soft reset is required to enable the new firmware.

If both the Slave and Master MP require reset, soft reset the Slave MP first (menu option 4) followed by the Master MP (menu option 3). After the Master MP is soft reset, the telnet session will be lost. Loss of the telnet session requires a **Ctrl-]** command (simultaneous *Control* and *Right Bracket* keys) to exit the MP Menu.

To reset the MP:

```
MP:CM> xd

    MP Diagnostics and Reboot menu
    ------------------------------
        1. Parameters checksum
        2. Ping
        3. Soft Reset the Master MP
        4. Soft Reset the Slave MP


Enter your choice:
```

Step 6 Re-establish the telnet session
Verify the MP revisions using the **sysrev** command:

```
MP:CM> sysrev

    Cabinet FPGA and Firmware revision report

System Backplane :  GPM     FM     OSP
                    ---     ---    ---
                   1.002   1.002  1.001

PCI Backplane    : LPM     HS
                    ---     ---
                   1.002  1.000

             LPM    BOB    Drain   SINC    PDC
             ---    ---    -----   ----    ---
CELL 0 :    2.002  1.000   1.000   2.002   16.011
CELL 1 :    2.002  1.000   1.000   2.002   16.011
CELL 2 :    2.002  1.000   1.000   2.002   16.011
CELL 3 :    2.002  1.000   1.000   2.002   16.011

                   FPGA     MP
                   ----     --
Master Core IO  : 1.001    4.022
Slave  Core IO  : 1.001    4.022
```

Step 7 Updating the remaining entities.
Launch the Firmware Update Utility:

```
MP:CM> fw
```

Step 8 In either single or dual partition configurations, the 2 entities (PDC, SINC,) should be updated during the same session. For this reason, all firmware files should reside in the same path.

Example if using Laptop:

\dist\version6_4

Enter the following information when prompted (an example of the Firmware Update Utility screen follows):

Enter the Entities to be upgraded: **Select the appropriate entity/entities to be upgraded.**

Enter your user name: **anonymous**

Enter your user password: **Enter your e-mail address**

Enter the ip address where the firmware can be found: **Enter the address of the anonymous FTP server.**

Enter the path where the firmware can be found: **Enter the directory path (for example, /dist/version6_4 or some other location). Do not list the actual firmware image filenames in this path.**

Enter the filename(s) of the firmware image(s): **For example, if the PDHC/SINC firmware image is *sinc204.bin*, enter sinc204.bin. Note that if you selected more than one entity type, you will be asked for more than one filename. Enter the appropriate image name for each entity type.**

Are you sure that you want to continue (Y/N): **y**

```
MP:CM> fw

    ********************************************************************
    *****                                                          *****
    *****                  Firmware Update Utility                 *****
    *****                                                          *****
    *****       (C) Copyright 2001 Hewlett-Packard Company         *****
    *****                    All Rights Reserved                   *****
    *****                                                          *****
    *****        THIS PROGRAM IS NOT LICENSED TO CUSTOMERS         *****
    *****                                                          *****
    *****  This program is intended for use by trained HP support  *****
    *****  personnel only.  HP shall not be liable for any damages *****
    *****  resulting from unauthorized use of this program.  This  *****
    *****  program is the property of HP.                          *****
    *****                                                          *****
    *****                      Version  3.02                       *****
    *****                                                          *****
    ********************************************************************

                                Protection  Flash       Current
  Number  Cabinet    Name       Domain     Handle   Firmware Version  Comments
  ------ --------- -------- ---------- -------- ------------------ --------
(1)  1         0     MP 0          0        0          4.022       Master
(1)  2         0     MP 1          1        1          4.022       Slave
     3         0   PDHC 0          0      256          2.002          -
     4         0    PDC 0          0      320         16.011          -
     5         0   PDHC 1          1      257          2.002          -
     6         0    PDC 1          1      321         16.011          -
(2)  7         0   PDHC 2         -1      258          2.002          -
(2)  8         0    PDC 2         -1      322         16.011          -
(2)  9         0   PDHC 3         -1      259          2.002          -
(2)  10        0    PDC 3         -1      323         16.011          -

(1) on the rp7410/rp7405 server the Master MP is MP1
(2) these entities will only be seen on the rp8400
*  A Production Domain value of –1 indicates that these cells do not belong to a partition
```

```
Enter the Entities to be upgraded (Ex: 3,4,10) : 3,4,5,6,(7,8,9,10)
Enter your user name: anonymous
Enter your user password:
Enter the ip address where the firmware can be found: 192.1.1.1
Enter the path where the firmware can be found: /dist/version6_4
Enter the filename of the firmware image for the PDHC: sinc204.bin
Enter the filename of the firmware image for the PDC: pdc17.9.bin
Are you sure that you want to continue(Y/N): y
```

Step 9 Following an update; it is necessary to verify that all entities selected were updated successfully. A successful update returns the following message:

```
Firmware Update has completed successfully for all entities.
MP:CM>
```

An unsuccessful update results in an error message. If the FTP connection was successful, but the update failed, a warning will be received for the entity being updated. For example:

```
Firmware Update failed for entity PDC 0.
DO NOT REBOOT PDC 0 until it has been successfully updated!!!
Firmware Update completed with errors.
```

Re-perform the firmware update procedure immediately for all entities failing to update successfully.

Step 10 Upon successful completion of SINC a soft reset is required. PDC upgrades do not require reset.

Step 11 Reset the SINC by selecting option H under the RU command, and entering each cell number individually:

```
MP:CM> ru

This command resets the selected MP bus device.

    B - BPS  (Bulk Power Supply)
    A - PACI (Partition Console Interface)
    G - MP   (Management Processor)
    H - PDHC (Cell Board Controller)
        Select device: h
    Enter cell number: 0

    Do you want to reset the Cell PDH Controller Slot 0? (Y/[N]) y

    -> The selected MP bus device will be reset.

MP:CM>
```

Note: Remember to repeat this step for ALL cell boards.

Step 12 Reset the partition(s) using the RS command:

```
MP:CM> rs

This command resets the selected partition.

WARNING: Execution of this command irrecoverably halts all
system processing and I/O activity and restarts the selected
partition.


Part#  Name
-----  ----
   0)  Partition 0
   1)  Partition 1

    Select a partition number: 0 (or 1)
```

Note: If more than one partition is configured, they both must be reset.

Step 13 Verify the system revision using the **sysrev** command:

```
MP:CM> sysrev

    Cabinet FPGA and Firmware revision report

System Backplane :  GPM     FM     OSP
                    ---     ---    ---
                   1.001   1.001  1.001

PCI Backplane    : LPM     HS
                    ---     ---
                   1.002  1.000

             LPM    BOB    Drain   SINC    PDC
             ---    ---    -----   ----    ---
CELL 0 :    2.002  1.000   1.000   2.004   17.009
CELL 1 :    2.002  1.000   1.000   2.004   17.009
CELL 2 :    2.002  1.000   1.000   2.004   17.009
CELL 3 :    2.002  1.000   1.000   2.004   17.009

                  FPGA     MP
                  ----     --
Master Core IO  : 1.001    4.022
Slave  Core IO  : 1.001    4.022
```

rp8400 / rp7410 / rp7405 FPGA Firmware Update Procedure Using the Onboard Scan Programming (OSP) Utility

Note 1: The FPGA firmware update process requires file transfer via FTP session. In the event that a loss of FTP session occurs, and the source of the interruption is corrected within approximately 3 minutes (for example, a removed LAN cable is re-inserted), the Onboard Scan Programming Utility will continue automatically with no loss of data.

The FPGA Upgrade procedure also requires that AC power be removed from the server to enable the new firmware, be sure to have Auto Boot turned off prior to beginning the upgrade. Verify BCH Path Flags or use the HP-UX command "**setboot –b off** " BEFORE shutting down the OS.

For interruptions greater than approximately 3 minutes, the Utility will timeout and end, returning the user to the command menu prompt:

```
Command interface inactivity timeout.  Aborting command.

MP:CM>
```

In the case of a timeout and incomplete FPGA firmware update, the user must restart the FPGA firmware update. DO NOT PERFORM ANY SORT OF RESET, OR POWER CYCLE, UNTIL THE FIRMWARE IS SUCCESSFULLY UPDATED.

Note 2: In past releases of firmware versions, all firmware files ended with a ".bin" extension. Starting at Version 6.0 release, there is a mixture of firmware files ending with ".bin" and ".osp" extension along with the first portion of the file name consistency changing slightly.

Step 1 **rp8400** users updating to Version 6.4 from Version 1.0 or 2.0, the following restrictions exist for FPGA firmware updates:

- Users updating to Version 6.4 from Version 1.0 or 2.0 must first update PDC, SINC, and MP to firmware Version 4.0/4.11 prior to performing commands with the OSP Utility.
- With PDC, SINC, and MP updated to Version 6.4, the System Backplane OSP FPGA must be updated to Version 4.0/4.11 prior to subsequent FPGA firmware updates.
- Following the OSP FPGA update, an AC power cycle is required. Users with multi-partition configurations should note that power must be cycled for all partitions.

Step 2 With power *on* to the machine and the Operating System shut down, place the partition(s) in the necessary state for the firmware to be updated. Reset the partition to stop at Boot is Blocked (BIB) for the rp8400 and to BCH for the rp7410/rp7405 by:

rp8400:

```
MP:CM> rr

This command resets for reconfiguration the selected partition.

WARNING: Execution of this command irrecoverably halts all system
         processing and I/O activity and restarts the selected
         partition in a way that it can be reconfigured.


  Part#  Name
  -----  ----
     0)  Partition 0

    Select a partition number: 0

    Do you want to reset for reconfiguration partition number 0?
   (Y/[N]) y

    -> The selected partition will be reset for reconfiguration.
MP:CM>
```

Note: if more then one partition they must all be at BIB

rp7410/rp7405:

```
MP:CM> rs

This command resets the selected partition.

WARNING: Execution of this command irrecoverably halts all
system processing and I/O activity and restarts the selected
partition.


  Part#  Name
  -----  ----
     0)  Partition 0

    Select a partition number: 0

    Do you want to reset partition number 0? (Y/[N]) y

   -> The selected partition will be reset.
```

Note: if more than one partition they must all be at BCH

Step 3 Launch the Onboard Scan Programming Utility:

```
MP:CM> osp
```

Step 4 rp8400 users updating to Version 6.4 from Version 1.0 or 2.0, the OSP FPGA must be updated first. Enter the following information when prompted (an example of the Onboard Scan Programming Utility screen follows):

Note: Additional information is available in the "Firmware Update Information, Precautions and Warnings" as well as "Revisions to this Document" sections. These sections assist understanding when the OSP FPGA must be updated first.

Enter the Entities to be upgraded: **Select the appropriate entity/entities to be upgraded.**

Enter your user name: **anonymous**

Enter your user password: **Enter your e-mail address**

Enter the ip address where the firmware can be found: **Enter the address of the anonymous FTP server.**

Enter the path where the firmware can be found: **Enter the directory path (for example, /dist/version6_4 or some other location). Do not list the actual firmware image filenames in this path.**

Enter the filename(s) of the firmware image(s): **For example, if the OSP FPGA firmware image is *osp_1.2.0b.osp,* enter *osp_1.2.0b.osp.* Note that if you selected more than one entity type, you will be asked for more than one filename. Enter the appropriate image name for each entity type.**

Are you sure that you want to continue (Y/N): **y**

```
**********************************************************************
*****                                                            *****
*****            Onboard Scan Programming Utility                *****
*****                                                            *****
*****       (C) Copyright 2001 Hewlett-Packard Company           *****
*****                   All Rights Reserved                      *****
*****                                                            *****
*****        THIS PROGRAM IS NOT LICENSED TO CUSTOMERS           *****
*****                                                            *****
*****  This program is intended for use by trained HP support    *****
*****  personnel only.  HP shall not be liable for any damages   *****
*****  resulting from unauthorized use of this program.  This    *****
*****  program is the property of HP.                            *****
*****                                                            *****
*****                      Version  1.00                         *****
*****                                                            *****
**********************************************************************

                          Protection  Flash      Current
Number  Cabinet    Name     Domain    Handle   FPGA Version
------ --------- -------- ---------- -------- --------------
(1)  1         0    CIO 0          0     2048      1.000
```

```
(1)  2          0    CIO 1          1     2049      1.000
     3          0      GPM          0     2184      1.000
     4          0       FM          0     2192      1.001
     5          0      OSP          0     2232      1.001
     6          0   Pci HS          0     2328      1.000
     7          0   PciLPM          0     2352      1.000
     8          0   Bob  0          0     2464      1.000
     9          0   Drain0          0     2472      1.000
    10          0   LPM  0          0     2480      2.001
    11          0   Bob  1          1     2465      1.000
    12          0   Drain1          1     2473      1.000
    13          0   LPM  1          1     2481      2.001
(2) 14          0   Bob  2          0     2466      1.000
(2) 15          0   Drain2          0     2474      1.000
(2) 16          0   LPM  2          0     2482      2.001
(2) 17          0   Bob  3          1     2467      1.000
(2) 18          0   Drain3          1     2475      1.000
(2) 19          0   LPM  3          1     2483      2.001
```

(1) the CIO files are different for the rp8400 and rp7410/rp7405
(2) these entities will only be seen on the rp8400

```
Enter the Entities to be upgraded (Ex: 2,4,7) : 5
Enter your user name: anonymous
Enter your user password:
Enter the ip address where the FPGA image file can be found: 192.1.1.1
Enter the path where the file(s) can be found: /dist/version6_4
Enter OSP controller FPGA image filename: osp_1.2.0b.osp
Are you sure that you want to continue(Y/N): y
```

DO NOT RESET the server unless you have received confirmation that the FPGA was updated successfully. Re-perform the firmware update procedure immediately for all entities failing to update successfully.

Step 5 Following OSP FPGA update, shutdown 48V power to the machine by the front power switch or the PE command:

```
MP:CM> pe

This command controls power enable to a hardware device.

    T - Cabinet
    C - Cell
    P - IO Chassis
        Select Device: t

    The power state is ON for Cabinet 0.
    In what state do you want the power? (ON/OFF) off

MP:CM>
```

Step 6 Cycle AC power to the rp8400 or rp7410/rp7405 by removing AC power cords, waiting approximately 30 seconds, then reinserting the cords.

Step 7 Restore power to 48V standby by the front power switch or the PE command:

```
MP:CM> pe

This command controls power enable to a hardware device.

    T - Cabinet
    C - Cell
    P - IO Chassis
        Select Device: t

    The power state is OFF for Cabinet 0.
    In what state do you want the power? (ON/OFF) on

MP:CM>
```

Step 8 Verify the OSP FPGA revision using the **sysrev** command.

```
MP:CM> sysrev

    Cabinet FPGA and Firmware revision report

System Backplane :  GPM     FM     OSP
                    ---     ---    ---
                    1.000   1.001  1.002

PCI Backplane    :  LPM     HS
                    ---     ---
                    1.000   1.000

            LPM    BOB     Drain    SINC    PDC
            ---    ---     -----    ----    ---
CELL 0 :    2.001  1.000   1.000    2.004   17.009
CELL 1 :    2.001  1.000   1.000    2.004   17.009
CELL 2 :    2.001  1.000   1.000    2.004   17.009
CELL 3 :    2.001  1.000   1.000    2.004   17.009

                   FPGA     MP
                   ----     ---
Master Core IO  : 1.000    4.022
Slave  Core IO  : 1.000    4.022
```

Step 9 Updating the remaining FPGAs.

Note 1: In past releases of firmware versions, all firmware files ended with a ".bin" extension. Starting at Version 6.0 release, there is a mixture of firmware files ending with ".bin" and ".osp" extension along with the first portion of the file name consistency changing slightly.

Note 2: rp8400 Cell board FPGA updates require a scree board (HP P/N 1253-5394) mounted on connector J-22 of the System Backplane board. The Bob, Drain and Pci HS FPGA's will not be updated.

- Launch the Onboard Scan Programming Utility:

```
MP:CM> osp
```

Enter the following information when prompted (an example of the Onboard Scan Programming Utility screen follows):

Enter the Entities to be upgraded: **Select the appropriate entity/entities to be upgraded.**

Enter your user name: **anonymous**

Enter your user password: **Enter your e-mail address**

Enter the ip address where the firmware can be found: **Enter the address of the anonymous FTP server.**

Enter the path where the firmware can be found: **Enter the directory path (for example, /dist/version6_4 or some other location). Do not list the actual firmware image filenames in this path.**

Enter the filename(s) of the firmware image(s): **For example, if the OSP FPGA firmware image is *celllpm_2.2.0b.osp*, enter *celllpm_2.2.0b.osp*. Note that if you selected more than one entity type, you will be asked for more than one filename. Enter the appropriate image name for each entity type.**

Are you sure that you want to continue (Y/N): **y**

```
*********************************************************************
*****                                                           *****
*****            Onboard Scan Programming Utility               *****
*****                                                           *****
*****       (C) Copyright 2001 Hewlett-Packard Company          *****
*****                   All Rights Reserved                     *****
*****                                                           *****
*****        THIS PROGRAM IS NOT LICENSED TO CUSTOMERS          *****
*****                                                           *****
*****  This program is intended for use by trained HP support   *****
*****  personnel only.  HP shall not be liable for any damages  *****
*****  resulting from unauthorized use of this program.  This   *****
*****  program is the property of HP.                           *****
*****                                                           *****
*****                      Version  1.00                        *****
*****                                                           *****
*********************************************************************
                          Protection  Flash      Current
 Number  Cabinet    Name     Domain    Handle   FPGA Version
 ------ --------- -------- ---------- -------- --------------
(1)  1         0    CIO 0          0     2048      1.001
(1)  2         0    CIO 1          1     2049      1.001
     3         0      GPM          0     2184      1.002
     4         0       FM          0     2192      1.002
     5         0      OSP          0     2232      1.002
     6         0   Pci HS          0     2328      1.000
     7         0   PciLPM          0     2352      1.002
     8         0   Bob  0          0     2464      1.000
     9         0   Drain0          0     2472      1.000
    10         0   LPM  0          0     2480      2.002
    11         0   Bob  1          1     2465      1.000
    12         0   Drain1          1     2473      1.000
    13         0   LPM  1          1     2481      2.002
(2) 14         0   Bob  2          0     2466      1.000
(2) 15         0   Drain2          0     2474      1.000
(2) 16         0   LPM  2          0     2482      2.002
```

```
 (2) 17         0   Bob  3          1     2467      1.000
 (2) 18         0   Drain3          1     2475      1.000
 (2) 19         0   LPM  3          1     2483      2.002
```

(1) the CIO files are different for the rp8400 and rp7410/rp7405
(2) these entities will only be seen on the rp8400

```
Enter the Entities to be upgraded (Ex: 2,4,7) : 1,2,3,4,6,7,9,10,12,
(if needed) (13,15,16,18,19)
Enter your user name: anonymous
Enter your user password:
Enter the ip address where the FPGA image file can be found: 192.1.1.1
Enter the path where the file(s) can be found: /dist/version6_4
Enter System Backplane Global Power Monitor FPGA image filename:
gpm_1.2.0b.osp
Enter System Backplane Fan Monitor FPGA image filename: sysfm_1.2.0b.osp
Enter PCI Backplane Local Power Monitor FPGA image filename:
pcilpm_1.2.0b.osp
Enter PCI Backplane Hot Swap FPGA image filename: pcihs_1.0.0b.osp
Enter Cell Board Local Power Monitor FPGA image filename:
celllpm_2.2.0b.osp
Enter Drain (PDH riser) FPGA image filename: drain_1.1.0b.osp
Enter Core IO FPGA image filename: rp8400 use cio_2.8.0b.osp or
rp7410/rp7405 use matcio_2.8.0b.osp
Are you sure that you want to continue(Y/N): y
```

DO NOT RESET the server unless you have received confirmation that the FPGAs were updated successfully. Re-perform the firmware update procedure immediately for all entities failing to update successfully.

Step 10 Following successful update, shutdown 48V power to the machine by the front power switch or the PE command:

```
MP:CM> pe

This command controls power enable to a hardware device.

    T - Cabinet
    C - Cell
    P - IO Chassis
        Select Device: t

    The power state is ON for Cabinet 0.
    In what state do you want the power? (ON/OFF) off

MP:CM>
```

Step 11 Cycle AC power to the rp8400/rp7410/rp7405 by removing AC power cords, waiting approximately 30 seconds, then reinserting the cords.

Step 12 Restore power to 48V by the front power switch or the PE command:

```
MP:CM> pe

This command controls power enable to a hardware device.

    T - Cabinet
```

```
    C - Cell
    P - IO Chassis
        Select Device: t

    The power state is OFF for Cabinet 0.
  In what state do you want the power? (ON/OFF) on
```

Step 13 Verify FPGA revisions using the **sysrev** command.

```
MP:CM> sysrev

    Cabinet FPGA and Firmware revision report

System Backplane : GPM     FM     OSP
                   ---     ---    ---
                   1.002   1.002  1.002

PCI Backplane    : LPM     HS
                   ---     ---
                   1.002   1.000

            LPM    BOB     Drain    SINC    PDC
            ---    ---     -----    ----    ---
CELL 0 :    2.002  1.000   1.001    2.004   17.009
CELL 1 :    2.002  1.000   1.001    2.004   17.009
CELL 2 :    2.002  1.000   1.001    2.004   17.009
CELL 3 :    2.002  1.000   1.001    2.004   17.009

                   FPGA     MP
                   ----     ---
Master Core IO  : 2.008    4.022
Slave  Core IO  : 2.008    4.022
```

Step 14 Reset the partition(s) using the RS command:

```
MP:CM> rs

This command resets the selected partition.

WARNING: Execution of this command irrecoverably halts all
system processing and I/O activity and restarts the selected
partition.


Part#  Name
-----  ----
   0)  Partition 0
   1)  Partition 1

    Select a partition number: 0 (or 1)
```

Step 15 You may now turn autoboot and autosearch back on at the BCH Configuration menu by setting the Path Flags to the proper settings or use the HP-UX command:

```
# setboot –b on
# setboot –s on
```

Server Expansion Unit (SEU) Firmware Update Procedure

Currently the only component in an SEU that may need updating is the MP.

1. Verify presence of MP's in an SEU as well as the power ok status of the components in cabinet 8 using the PS command:

Note: When a SEU is connected to an rp8400 system, cabinet id 8 will be assigned to the SEU.

```
MP:CM> ps

Display detailed status of the selected MP bus device.
```

```
The following MP bus devices were found:
+---+----+-----+-------+-------+-----------+
|   |    |     |       |       |           |
|   |    | Sys |       |  IO   | Bulk Pwr  |
|Cab| MP |Bkpln| Cells |Chassis| Supplies  |
| # |M  S|     |0 1 2 3| 0   1 |0 1 2 3 4 5|
+---+----+-----+-------+-------+-----------|
| 0 |*  *|  *  |* * * *| *   * |* * * * * *|
| 8 |*  *|  *  |- - - -| *   * |* * - - - -|
+---+----+-----+-------+-------+-----------+

You may display detailed power and hardware status for the
following items:

    T - Cabinet
    S - System Backplane
    G - MP (Core I/O)
    P - IO Chassis
    C - Cell
        Select Device: t

    Enter cabinet number (0 or 8): 8

HW status for rp8400 IO cabinet : NO FAILURE DETECTED

Power switch is on
Right Door is closed
Top Door is closed
Left Door is closed

Total Power Available 2000 VA
Total Power Needed 905 VA
Power Redundancy : redundant
Power Viability : viable



 Power Status
---------------+-----+-------+-----+
               |     |       |     |
               | Sys |  IO   |     |
               |Bkpln|Chassis| BPS |
               |     | 0   1 | 0 1 |
---------------+-----+-------+-----|
 Populated     |  *  | *   * | * * |
 Enabled       |  *  | *   * | * * |
 Power OK      |  *  | *   * | * * |
 Warning/Fault |     |       |     |
 Attention LED |     |       |     |
```

2. Update the MP firmware in the SEU.

```
MP:CM> fw

    ********************************************************************
    *****                                                          *****
    *****                  Firmware Update Utility                 *****
    *****                                                          *****
    *****       (C) Copyright 2001 Hewlett-Packard Company         *****
    *****                   All Rights Reserved                    *****
    *****                                                          *****
```

```
*****        THIS PROGRAM IS NOT LICENSED TO CUSTOMERS          *****
*****                                                           *****
*****  This program is intended for use by trained HP support   *****
*****  personnel only.  HP shall not be liable for any damages  *****
*****  resulting from unauthorized use of this program.  This   *****
*****  program is the property of HP.                           *****
*****                                                           *****
*****                      Version  3.02                        *****
*****                                                           *****
*****************************************************************

                                        Flash        Current
 Number  Cabinet    Name   Partition  Handle   Firmware Version  Comments
 ------ --------- -------- --------- -------- ----------------- --------
     1         0     MP 0         0        0          4.022      Master
     2         0     MP 1         1        1          4.022      Slave
     3         8     MP 0         0    32768          4.020      Master
     4         8     MP 1         1    32769          4.020      Slave
     5         0   PDHC 0         0      256          2.004         -
     6         0    PDC 0         0      320         17.009         -
     7         0   PDHC 1         1      257          2.004         -
     8         0    PDC 1         1      321         17.009         -
     9         0   PDHC 2         2      258          2.004         -
    10         0    PDC 2         2      322         17.009         -
    11         0   PDHC 3         3      259          2.004         -
    12         0    PDC 3         3      323         17.009         -

Enter the Entities to be upgraded (Ex: 3,4,10) : 3,4
Enter your user name: anonymous
Enter your user password:
Enter the ip address where the firmware can be found: 192.1.1.1
Enter the path where the firmware can be found: /dist/version6_4
Enter the filename of the firmware image for the MP: MP_A.4.22.0.bin
Are you sure that you want to continue(Y/N): y
```

3. Continue with the remaining portion of the firmware upgrade by proceeding with step 3 of the "rp8400 / rp7410 / rp7405 Firmware Update Procedure Using the Firmware (FW) Update Utility" section. Below is a sysrev output of a 4 cell rp8400 system with a SEU attached after a successful firmware update to version 6.4.

```
MP:CM> sysrev

Cabinet FPGA and Firmware revision report

System Backplane :   GPM          FM        OSP
                   -------     -------    -------
                     1.002       1.002      1.002

PCI Backplane    :   LPM          HS
```

```
                    -------     -------
                      1.002       1.000

              LPM         BOB       DRAIN       PDHC       PDC
            -------     -------     -------     -------     -------
CELL 0 :      2.002       1.000       1.001       2.004      17.009
CELL 1 :      2.002       1.000       1.001       2.004      17.009
CELL 2 :      2.002       1.000       1.001       2.004      17.009
CELL 3 :      2.002       1.000       1.001       2.004      17.009

                     FPGA          MP
                   -------      -------
Master Core IO  :    2.008        4.022
Slave  Core IO  :    2.008        4.022


IO Cabinet FPGA and Firmware revision report

System Backplane :   GPM           FM         OSP
                    -------      -------     -------
                      1.002        1.002       1.002

PCI-X Backplane  :   LPM           HS
                    -------      -------
                      2.000        1.000

                        FPGA          MP
                      -------      -------
IOX Master Core IO  :   2.008        4.022
IOX Slave  Core IO  :   2.008        4.022
```